

**REMARKS**

Claims 1-28 are pending in this application. Claims 1-14 are rejected. Claims 1, 3, 13 and 14 are amended herein. Attached hereto is a marked-up version of the changes made by the current amendment, captioned "Version with Markings to Show Changes Made." No new matter has been added.

**Rejections under 35 U.S.C. §103(a)**

*Claims 1-12 are rejected under 35 U.S.C. §103(a) as being unpatentable over JP 2000-28696 to Hiyama et al. in view of U.S. Patent 5,998,236 to Roeder et al. Claims 13 and 14 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kanaya et al. (U.S. Pub. 2002/0063274) in view of Roeder et al.*

Applicants respectfully disagree with the rejections, in light of the present clarifying amendments. Applicants note that the claimed inventions comprise a buffer structure formed beneath the lower electrode or the lower electrode that has a height larger than a width thereof. According to this feature, in ferroelectric film formation process, the influence of the stress due to the thermal expansion coefficient difference between the substrate and the ferroelectric film can be suppressed, whereby the ferroelectric film having a crystal oriented substantially perpendicular to a surface of the lower electrode can be formed.

As described on page 15, line 2 to page 17, line 3 of the present application, the thermal expansion coefficient difference between the substrate and the ferroelectric film is very influential to the orientation of the ferroelectric film. For example, when the PZT film is formed over the Si

substrate, the PZT film has (100) orientation. When the PZT film is formed over the MgO substrate, the PZT film has (001) orientation. On the other hand, when the buffer structure or the lower electrode having a height larger than a width thereof is formed beneath the ferroelectric film, the stress due to the thermal expansion coefficient difference between the ferroelectric film and the substrate can be absorbed by the buffer structure or the lower electrode. Accordingly, the ferroelectric film has an orientation that depends on an orientation of the lower electrode, whereby a capacitor comprising a ferroelectric film oriented substantially perpendicular to a surface of the lower electrode can be stably formed.

Applicants submit that neither Hiyama et al., Kanaya et al., nor Roeder et al. teach or suggest the structure for suppressing the stress induced in the ferroelectric film by the substrate. Hiyama et al., Kanaya et al., and Roeder et al. neither teach nor suggest the buffer structure or the lower electrode having a height larger than a width thereof.

Therefore, Applicants submit that Hiyama et al., Kanaya et al., and Roeder et al. are clearly different from the present invention and do not provide any motivation for the present invention. Thus, claims 1-14 would not have been obvious to one of ordinary skill in the art.

For at least the above reasons, Applicants submit that the present amendments overcome the rejections of record. Applicants earnestly request that the claims be passed to issue.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Amendment under 37 C.F.R. 1.111  
Masaki KURASAWA et al.

U.S. Patent Application Serial No. 09/960,398  
Attorney Docket No. 011254

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees that may be due with respect to this paper to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP

  
Kenneth H. Salen  
Attorney for Applicants  
Reg. No. 43,077

KHS/plb  
Atty. Docket No. **011254**  
Suite 1000, 1725 K Street, N.W.  
Washington, D.C. 20006  
(202) 659-2930



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Enclosures: Version with Markings to Show Changes Made

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE CLAIMS:**

**Please amend claims 1, 3, 13 and 14 as follows:**

1. (Amended) A capacitor comprising:

a buffer structure formed on a substrate, the buffer structure having a height larger than a width thereof;

a lower electrode formed on the buffer structure;

a capacitor dielectric film formed on the lower electrode, and formed of a perovskite ferroelectric material having a smaller thermal expansion coefficient than that of the buffer structure and having a crystal oriented substantially perpendicular to a surface of the lower electrode; and

an upper electrode formed on the capacitor dielectric film.

3. (Amended) A capacitor comprising:

a lower electrode formed on a substrate, the lower electrode having a height larger than a width thereof;

a capacitor dielectric film formed on the lower electrode, and formed of a perovskite ferroelectric material having a larger thermal expansion coefficient than that of the substrate and having a crystal oriented substantially perpendicular to a surface of the lower electrode; and

an upper electrode formed on the capacitor dielectric film.

13. (Amended) A semiconductor device comprising:

a memory cell transistor formed on a semiconductor substrate, and including a gate electrode, and source/drain diffused layers formed in the semiconductor substrate respectively on both sides of the gate electrode;

an insulation film covering the semiconductor substrate with the memory cell transistor formed on;

a buffer structure formed on the insulation film, the buffer structure having a height larger than a width thereof; and

a capacitor formed on the buffer structure, and including a lower electrode electrically connected to one of the source/drain diffused layers; a capacitor dielectric film formed on the lower electrode, and formed of a perovskite ferroelectric material having a smaller thermal expansion coefficient than that of the buffer structure and having a crystal oriented substantially perpendicular to a surface of the lower electrode; and an upper electrode formed on the capacitor dielectric film.

14. (Amended) A semiconductor device comprising:

a memory cell transistor formed on a semiconductor substrate and including a gate electrode, and source/drain diffused layers formed in the semiconductor substrate respectively on both sides of the gate electrode;

an insulation film covering the semiconductor substrate with the memory cell transistor formed on; and

a capacitor formed on the insulation film, and including a lower electrode electrically connected to one of the source/drain diffused layers, the lower electrode having a height larger than a width thereof; a capacitor dielectric film formed on the lower electrode, and formed of a perovskite ferroelectric material having a larger thermal expansion coefficient than that of the semiconductor substrate and having a crystal oriented substantially perpendicular to a surface of the lower electrode; and an upper electrode formed on the capacitor dielectric film.